REMARKS

Applicants respectfully request favorable reconsideration of this application.

Claims 105-118, and 130-143 are pending.

In the outstanding Office Action, Claims 105-118 and 130-143 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Schubert (U.S. 2003/30069724, hereinafter "*Schubert*") in view of Yalamanchili ("VHDL: From Simulation to Synthesis", hereinafter "*Yalamanchili*") and further in view of OrCAD ("OrCAD's Autorouter User's Guide", hereinafter "*OrCAD*"). Applicant respectfully traverses this rejection.

Claim 105 recites, *inter alia*, a computer system for automatically generating a simulation model, the simulation model comprising software simulation elements each corresponding to an integrated circuit under development, wherein the integrated circuits together comprise the design of a processing machine that conforms to a functional specification of the selected configuration as defined in the configuration definition file, and wherein the integrated circuits are not physically present in the processing machine.

It is apparent that the applied references fail to teach or suggest at least the above-recited features of Claim 105.

As acknowledged by the Office Action on page 3, Schubert fails to teach or suggest generating a simulation model comprising software simulation elements each corresponding to an integrated circuit under development, wherein the integrated circuits are not physically present in the processing machine. However, the Office Action alleges that both Yalamanchili and OrCAD remedy the deficiencies of Schubert. In particular, the Office Action relies on the top slide on page 7 of Yalamanchili and on the item marked "Auto DFM" on page 36 of OrCAD as allegedly disclosing generating a simulation model comprising software simulation elements each corresponding to an

integrated circuit under development, wherein the integrated circuits are not physically present in the processing machine. However, the cited portions of Yalamanchili and OrCAD fail to teach or suggest generating a simulation model comprising software simulation elements corresponding to an integrated circuit under development. In contrast, the cited portion of Yalamanchili describes a digital system design flow where simulation models are applied to verify the circuit design before manufacture, and the cited portion of OrCAD describes an auto-routing protocol to verify the circuit design before manufacture.

Thus, although Yalamanchili and OrCAD arguably teach performing simulation verification on integrated circuits prior to development, both fail to teach or suggest generating a simulation model comprising software elements corresponding to an integrated circuit under development, as recited in Claim 105. Additionally, although assuming arguendo that it could be obvious to apply a known simulation model to verify the design circuit before it is manufactured, as suggested by the Office Action on page 4, Applicant respectfully submits that it is not obvious to substitute applying a simulation model with generating a simulation model comprising software elements corresponding to an integrated circuit under development.

Therefore, the Applicant respectfully submits that Claim 105 distinguishes patentably from the applied references.

Claim 130 also recites, *inter alia*, generating a simulation model comprising software simulation elements each corresponding to an integrated circuit under development, wherein the integrated circuits together comprise the design of a processing machine that conforms to a functional specification of the selected configuration as defined in the configuration definition file, and that the integrated circuits are not physically present in the processing machine.

Therefore, Applicants respectfully submit that independent Claim 130 also distinguishes patentably from the applied references for at least the reasons discussed above with respect to Claim 105.

The remaining claims are also believed to be patentable due to their respective dependence from independent Claims 105 and 130, as well as for the additional features recited in the remaining claims.

In view of the foregoing, Applicants respectfully submit that this application is in condition for allowance. Accordingly, a prompt Notice of Allowance is respectfully solicited.

However, should the Examiner believe that any further action is necessary to place this application in better form for allowance the Examiner is invited to contact Applicant's representative at the telephone number listed below.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (T2147-908626) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

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